An ASIC dedicated to the RPCs' front-end of the dimuon arm trigger in the ALICE experiment

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Abstract

A first prototype of the front-end ASIC dedicated to the trigger detector of the dimuon arm of ALICE has been designed and tested.

This note introduces the new discrimination technique implanted in the chip in order to improve the time resolution of the Resistive Plate Chambers (RPC) in the streamer mode. The electronic design is then described and the test results are presented.

I. INTRODUCTION

The trigger system of the dimuon arm of the ALICE/LHC detector has to select events containing two muons from the decay of heavy resonances like J/Ψ or ϒ, amongst all background sources. The set up is composed of 72 Resistive Plate Chambers, a gaseous detector where the electrical charge produced by the crossing of a charged particle is collected on 1-4 cm wide, 35-70 cm long, strip lines. About 21000 readout channels are necessary to cover the whole detector area.

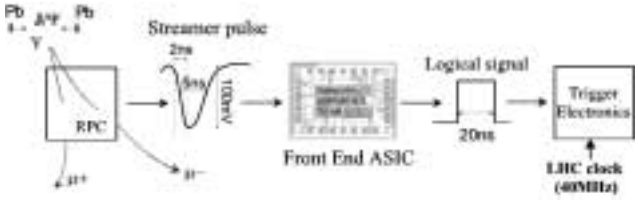

Figure 1: signal processing from detectors to trigger electronics

RPCs are operated in streamer mode in ALICE and no amplification of the analog signals picked up on the strips is needed. These signals are discriminated and then converted into a logical signal with a width of about 20 ns (figure 1). The resulting 21 000 channels "bit pattern" is sent in differential mode through 20m long cables to the trigger electronics. A sampling at the LHC clock frequency (40 MHz) is performed at this level before the dimuon trigger decision is issued.

Using conventional discrimination techniques, the time resolution is better when using RPC in avalanche mode (commonly 1ns), unless the RPC is operated in streamer mode at quite high running voltages that is not suitable [1]. In order to improve the time resolution in streamer mode, a new discrimination technique called "ADULT" has been studied.

II. THE "ADULT" DISCRIMINATION TECHNIQUE

This technique is described in details in [2]. Cosmic ray tests results are exposed. A 50x50cm^2 RPC, with 2mm wide gas gap and electrode resistivity of a few $10^{10}\Omega$.cm is used. Pulses are shown for a running high voltage of 9200V in streamer mode (figure 2).

The observation of the shape of these pulses indicates that the streamer signal itself is preceded by a smaller signal, called "avalanche precursor" . The streamer signal exhibits important time fluctuations while the avalanche precursor is almost steady.

The "ADULT" technique (**A DU**a**L T**hreshold) makes the most of this particular pulse shapes. It is based on the use of two discriminators, one with a low threshold (typically 10mV/50Ω) at the level of the avalanche precursor and the other with a high threshold (typically 80 mV/50Ω) at the level of the streamer. A coincidence of the two out coming signals is then performed. The one corresponding to the low threshold gives the time reference. The second one, outputted by the high threshold discriminator, is indispensable to keep

all the advantages of the streamer mode (better signal-to-noise ratio, cluster size,…).

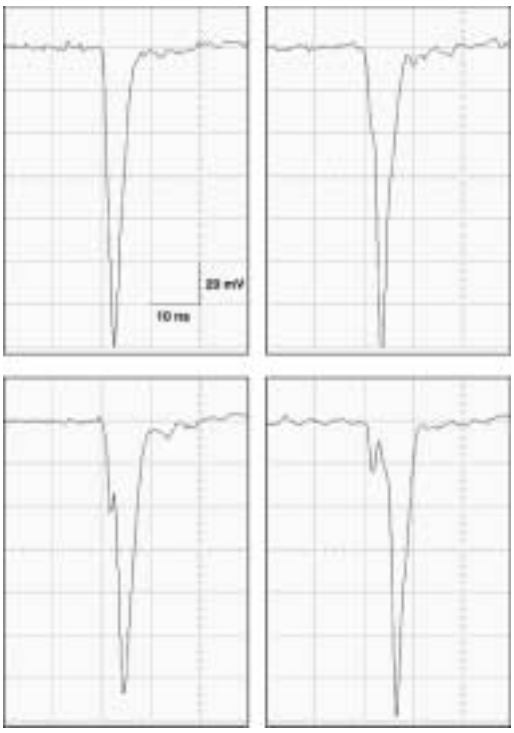

Figure 2: RPC pulse shape examples

III. DESIGN OF THE CHIP

A. General description

This dedicated discrimination technique has been implanted in the front-end chip developed at the "Laboratoire de Physique Corpusculaire" of Clermont-Ferrand. The chosen technology is AMS BiCMOS 0.8µm, well adapted to the design of fast comparators with low input offset voltage.

The prototype chip has only one channel. The "ADULT" discriminator stage is built with two fast comparators, and a delay followed by an "AND" gate (figure 3). The output signal of the low threshold comparator is delayed by 10ns, and then a coincidence with the high threshold one is done. This delay value has been chosen during cosmic ray tests [2], because it is not likely, in normal function condition, that the avalanche precursor comes earlier than 10ns relatively to the streamer. So the coincidence output is in time with the latest of the two input signals, namely the low threshold signal, as long as the delay between the precursor and the streamer is shorter than the 10ns delay value.

Additional functions are also implemented in the chip.

- An "one-shot" system prevents any channel from re-triggering during 100ns. When the high threshold comparator detects a streamer, its output activates a monostable. The monostable output state changes immediately and this level is held during about 100ns. The two comparators are blind during this time.

- A remote control delay, up to 50ns, common for a whole chip (i.e. eight channels in the final design) is tuned by an external DC voltage. It allows to adjust, if needed, the output timing of the signal.

- The signal is converted into a 20ns logical ECL level in order to drive a 20m twisted pair cable.

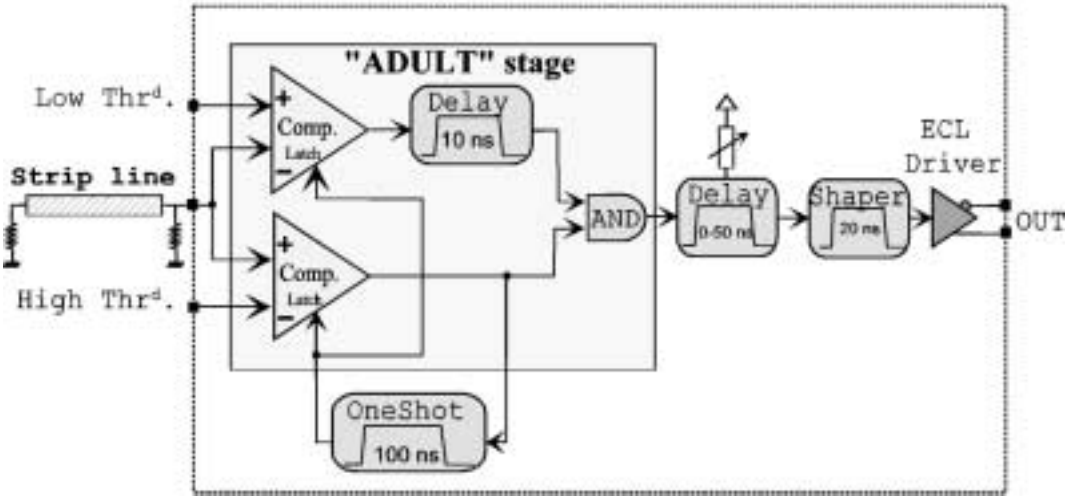

Figure 3: single channel block diagram

B. Comparators

The comparators are made of two differential amplification stages (figure 4), with a total gain of about 700 (57dB). The transistors chosen for this input stage are bipolar because of their relatively low threshold voltage dispersion comparatively to the MOS ones. The input noise has been studied. It is dominated by the thermal noise of the input transistors Q1 and Q2. The input noise voltage is lower than 100µV rms for the total frequency bandwidth.

The power consumption of each comparator is about 12mW.

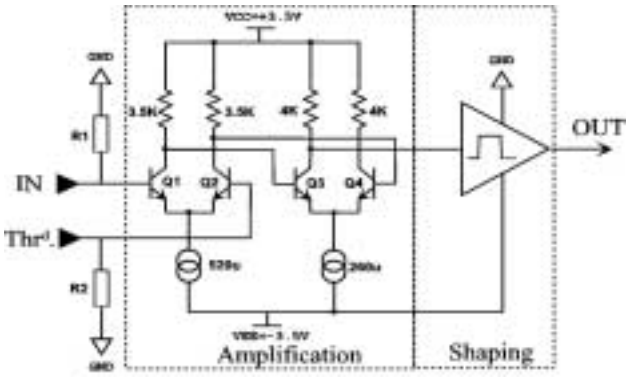

Figure 4: schematic diagram of the comparator

The amplifier is followed by a shaper in order to obtain a logical pulse well-matched to the next stage.

C. "Delay", "oneshot" and "shaper" stages

All these stages are built with simple monostables. A capacitor C is charged with a constant current Io (figure 5) until the voltage Vc reaches a DC threshold value (Vth). A pulse with a fixed width (function of the capacitor, current and threshold values) is outputted and can be used to realize the 10ns delay, the 100ns "oneshot" protection or the 20ns wide ECL signal. The capacitor is discharged with a PMOS transistor (Q) connected to the ground. The adjustable delay stage is obtained with an external control of the DC threshold value Vth.

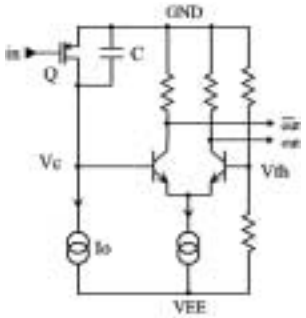

Figure 5: schematic diagram of a monostable stage

IV. LABORATORY TEST RESULTS

Five packaged chips were delivered in May 2000. The tests in laboratory were made with a pulse generator to simulate RPC signals, and with an oscilloscope differential probe (500MHz) connected to the output pins. They have shown that each stage of the chip works perfectly, as illustrated by the figures 6 to 9. The power consumption is still a little bit high (140mW per channel) but will be decreased in the future by replacing the ECL driver by a LVDS one.

The low threshold discriminator gives the time reference (figure 6) as long as the delay between the avalanche precursor and the streamer signals is less than 10ns, as explained previously. The high threshold discriminator selects only the big enough streamer pulses (figure 7).

The ECL output signal can be delayed in a range of about 60 ns (figure 9) and the "one-shot" protection (figure 8) is effective even though it is longer (138 ns) than the required value.

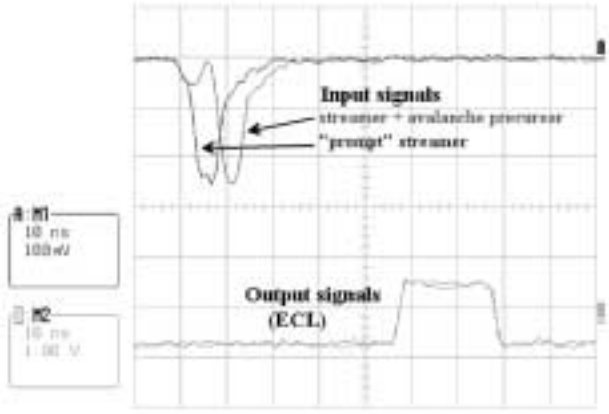

Figure 6: timing of the two output signals corresponding to a prompt streamer and a streamer preceded by an avalanche precursor.

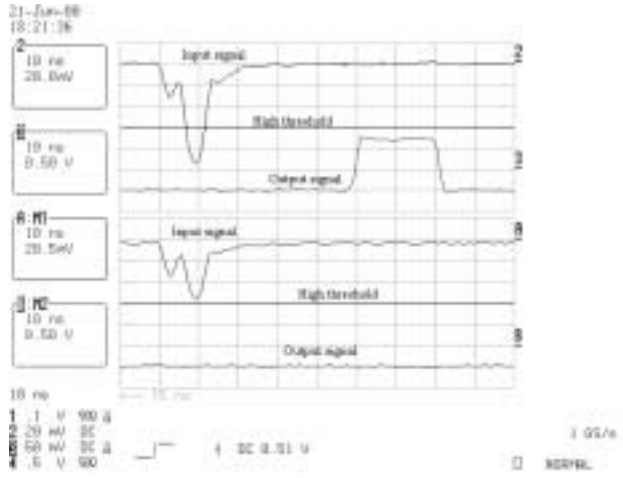

Figure 7: output signals for a pulse height respectively below and above the high threshold.

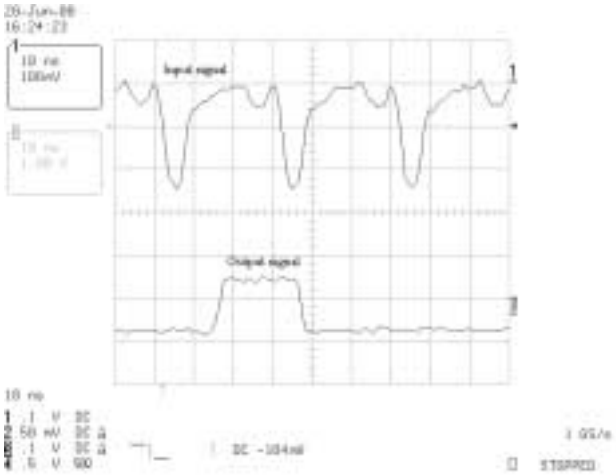

Figure 8: illustration of the "oneshot" protection.

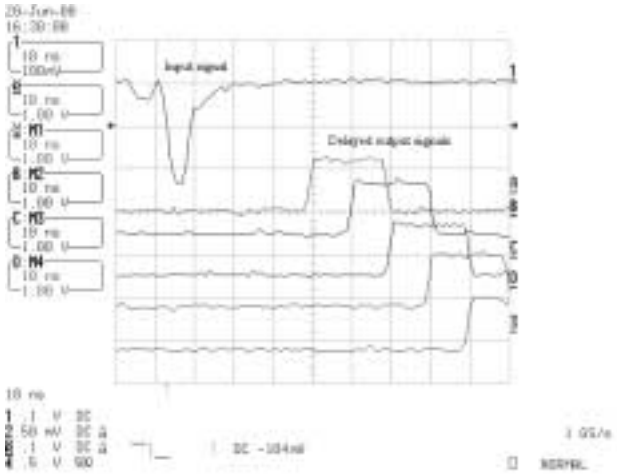

Figure 9: illustration of the possibility of delaying the output signal.

V. PRELIMINARY BEAM TEST RESULTS

A. The experimental set up

A RPC equipped with eight of these prototype chips has been tested at the CERN/PS beam area at the beginning of July 2000. A 50x50cm^2 RPC, with 2mm wide gas gap and electrode resistivity of a few $10^9\Omega$.cm was used. It was fluxed with a special gas mixture of Ar/i-C4H10/C2H2F4/SF6 in the respectively percentages of 44/7/40/4 which has been optimised in cosmic ray tests for out purpose.

The time resolution obtained with the "ADULT" technique has been compared to the one in case of single threshold discriminator. Sixteen vertical strips signals were discriminated by fast ECL comparators, with a single threshold fixed to the High Threshold value. The eight central horizontal strips of the same detector were equipped with the eight ASIC.

The time resolution is measured with three eight channels TDC (Time to Digital Converter) Camac modules (100ps resolution) installed in the control room. A coincidence between a scintillators (Sc.) hodoscope (3 vertical Sc. and 4 horizontal Sc.) positioned after the RPC and a "wide" Sc. placed before, provided the time reference called TRIGGER. This TRIGGER signal is used as the COMMON START pulse for the TDC modules. Three tracking chambers with a resolution of 2mm were also positioned on the beam axis, before and after the RPC. The "central flux" on the RPC was monitored by a coincidence of two scintillators (called "cross") covering an area of 4cm^2 where the incident flux is maximum.

B. Preliminary results

Figure 10 displays examples of time distribution obtained with the new chip (thresholds [10mV, 80mV]) (top plots) and with a single threshold [80mV] discriminator (bottom plots).

Two running HV values are considered: 9200V (left plots), where the RPC has a good efficiency (>98%) and 8600V (right plots) where the efficiency drops to about 60%. All the histograms are normalized to 1000 entries.

We observe a wide, double time structure with the single threshold discriminator. As expected, the time distribution with the "ADULT" ASIC does not exhibit this double structure at the running HV value (9200V). We obtain a very narrow time peak ($\sigma_T^{peak} \leq 1$ns). The insert in logarithmic vertical scale shows the small proportion of events in the tail (~2%).

At 8600V, the delay time between the avalanche precursor and the streamer signals may exceed 10ns. In this case, the time reference of the coincidence in the "ADULT" chip is given by the high threshold signal. This is the reason why a second peak appears in the time distribution at the right side of the first one. We note that this case occurs where the detector is not fully efficient which validates our choice of a delay of 10ns.

But the best way to compare the time resolution of the two electronics is to plot the efficiency curves for several time windows. The efficiency must be to its maximum when the signals from front end electronics are sampled at the LHC period of 25ns, including all possible time jitters, which requires better performances on a single channel. The right part of figure 11 gives the efficiency curves for a flux of 15Hz/cm^2. Two time windows have been considered: 25ns as previously and 8ns. For "ADULT", the efficiency is still good with the 8ns window which evidences the excellent time resolution and small time jitter versus HV. The situation is obviously different with a single threshold discriminator as indicated by the picture. It is also illustrated with the right plot of the figure 12, where the time resolutions are compared (σ_T rms in a 25ns window).

The efficiency curve in a 25ns window as a function of the local flux is summarized in the left part of the figure 11. The efficiency of the detector is still good for a local flux of 450Hz/cm^2 (the requirement is below 50Hz/cm^2 in ALICE [3]).

The cluster size distribution versus HV is plotted in figure 12 (left plot) for 2cm wide, 50cm long strips, and 15Hz/cm^2 local flux. As expected, exactly the same curve is obtained with single threshold discriminators set at the high threshold value. The results satisfy the requirements in ALICE [3].

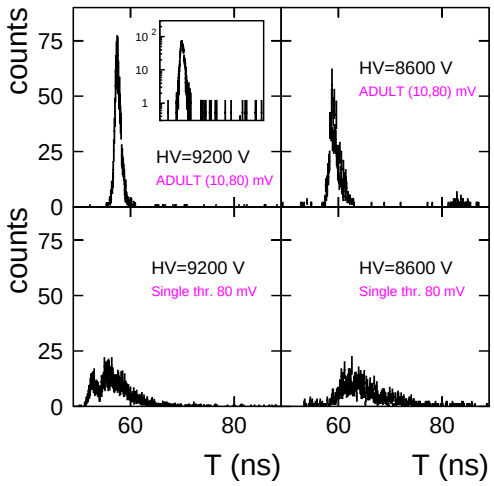

Figure 10: examples of time distribution with "ADULT" (top plots) compared with a single threshold discriminator (bottom plots)

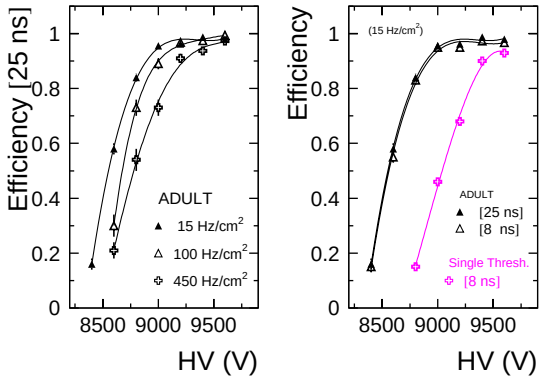

Figure 11: efficiency curve with "ADULT" at three flux (left plot), efficiency of the two electronics in two windows (25 and 8ns) (right plot)

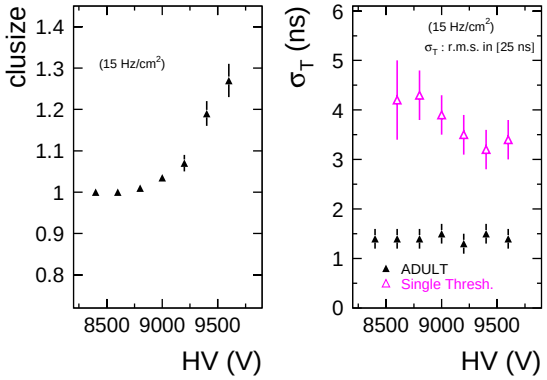

Figure 12: cluster size distribution (left plot) and time resolution (right plot)

VI. CONCLUSIONS

We have designed, prototyped and fully tested the first BiCMOS front-end ASIC prototype for the Resistive Plate Chambers of the dimuon arm in ALICE. As expected, the time resolution of the RPC in streamer mode is considerably improved with this enhanced electronics.

A new prototype has already been designed and will be tested in laboratory at the beginning of autumn 2000. The ECL output driver has been replaced by a LVDS one in order to reduce the power consumption to less than 100mW per channel. The final chip prototype with eight channels has to be designed during winter 2000. The full production (3000 chips) will be carry out during the year 2002.

VII. REFERENCES

[1]: A.Picotti et al., Nuclear Physics B (Proc. Suppl.) 78 (1999) 84-89

[2]: P.Dupieux et al., "A new discrimination technique to improve the time resolution of resistive plate chambers in streamer mode", NIM A, in press.

[3]: ALICE TDR 5 (Dimuon forward spectrometer), CERN/LHCC 99-22 (08/99) 143-208